R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a method of recovering from invalid data in a first register within a pipelined processor. The method generally comprises the steps of (A) setting a first status for the first register to an invalid state in response to a first data in the first register being invalid and (B) stalling the processor in response to both (i) an instruction requiring the first data and (ii) the first status being in the invalid state.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and the new claims may be found in the specification, for example, on page 7 lines 8-21, page 8 lines 15-21, page 11 lines 6-15, page 12 lines 8-14, page 13 lines 1-13 and FIGS. 3-5 as originally filed. Thus, no new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the title has been obviated by appropriate amendment and should be withdrawn.

The objection to the headings under 37 CFR 1.77(c) is respectfully traversed and should be withdrawn. Permissive language is used in 37 CFR 1.77(c) regarding bold and underlines.

As such, the headings as filed are compliant with the rule and the objection should be withdrawn.

IN THE DRAWINGS

The objection to the FIG. 5, reference number 506 has been obviated by submitting a replacement drawing showing the reference number 506 darker as requested by the Examiner. Approval of the replacement drawing is respectfully requested.

CLAIM OBJECTIONS

The objections to claims 1, 5, 8 and 12 for informalities have been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 7 and 14 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 3-6 and 15 under 35 U.S.C. §102(b) as being anticipated by Mirapuri et al. '294 (hereafter Mirapuri) is respectfully traversed and should be withdrawn.

Mirapuri concerns a method and apparatus for restarting pipeline processing (Title). Mirapuri does not appear to disclose or suggest every element as arranged in the claims. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides a step for setting first status for a first register to an invalid state in response to a first data in said first register being invalid. In contrast, Mirapuri appears to be silent regarding **data registers** having an invalid state. Furthermore, the arguments on page 4, paragraph 15a appear to be incorrect as column 9, lines 35-42 concern **instruction registers**. Since one of ordinary skill in the art of pipeline processors would consider instruction registers distinguishable from data registers, as evidenced by FIG. 4 of Mirapuri, the instruction registers of Mirapuri do not **expressly or inherently**[1] describe the claimed first register holding data. Therefore, Mirapuri does not appear to disclose or suggest setting first status for a first register to an invalid state in response to a first data in said first register being invalid as presently claimed.

Claim 1 further provides a step for stalling a processor in response to both (i) an instruction requiring a first data and (ii) a first status being in an invalid state. The argument on

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[1] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987).

page 5, paragraph 15b of the Office Action appears to be reversing a cause and an effect. Column 10, lines 55-65 of Mirapuri appear to indicate that **a pipeline overrun causes a stall** with a consequence that data remaining in the pipeline may be incorrect. In contrast, the **data being invalid causes the stall** in the claim. Furthermore, Mirapuri appears to be silent, and the Office Action makes no arguments, that the stall is also caused by an instruction requiring the data considered to be invalid. Therefore, Mirapuri does not appear to disclose or suggest stalling a processor in response to both (i) an instruction requiring a first data and (ii) a first status being in an invalid state as presently claimed. Claim 15 provides language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 15 provides a structure comprising a means for setting a first status to an invalid state in response to a first data in a means for buffering being invalid. In contrast, Mirapuri appears to be silent regarding any structure for setting status bits in data registers because Mirapuri appears to be silent regarding any data registers having status bits to set. Therefore, Mirapuri does not appear to disclose or suggest a structure comprising a means for setting a first status to an invalid state in response to a first data in a means for buffering being invalid as presently claimed.

Applicants' representative respectfully traverses the assertion on page 8, paragraph 20c that it is inherent to have a means to set every bit in a register. Inherency requires certainty of results, not mere possibility.[2] Since an 8-bit register holding a 7-bit ASCII character may leave the last (8^{th}) bit unused, no means to set the unused last bit is certain and thus cannot be inherent. As such, claim 15 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides setting a first status to an invalid state in response to a first register receiving a second data from a second register having a second status in the invalid state. Despite the assertion on page 5, paragraph 16 of the Office Action, the text in column 10, lines 56-58 of Mirapuri appears to be silent regarding setting a status if one register passes invalid data to another register. The cited text of Mirapuri merely states, "Often, the stall condition is only detected after parts of the pipeline have advanced using incorrect data." Nowhere in the quote, or in any other section, does Mirapuri expressly or inherently describe setting a status for a data register invalid. Therefore, Mirapuri does not appear to disclose or suggest setting a first status to an invalid state in response to a first register receiving a second data from a second register having a second

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[2] See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981).

status in the invalid state as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides buffering a first status as a plurality of bits to provide for multiple conditions that would indicate an invalid state. In contrast, Mirapuri appears to be silent regarding multiple status bits indicating an invalid state of data. Furthermore, page 7, paragraph 19 of the Office Action offers no evidence that the word "information" expressly or inherently mean multiple bits and thus is merely a conclusory statement. Therefore, Mirapuri does not appear to disclose or suggest buffering a first status as a plurality of bits to provide for multiple conditions that would indicate an invalid state as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 8 and 10-13 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Steiss '420 is respectfully traversed and should be withdrawn.

The rejection of claims 2 and 7 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Sites '167 is respectfully traversed and should be withdrawn.

The rejection of claims 9 and 14 under 35 U.S.C. §103(a) as being unpatentable over Mirapuri in view of Sites and Steiss is respectfully traversed and should be withdrawn.

Mirapuri concerns a method and apparatus for restarting pipeline processing (Title). Sites concerns ensuring data integrity by locked-load and conditional-store operations in a multiprocessor system (Title). Steiss concerns a microprocessor arithmetic logic unit using multiple number representations (Title). Mirapuri, Sites and Steiss, alone or in combination, do not appear to teach or suggest every element as claimed. Furthermore, *prima facie* obviousness has not been established to combine the references. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 8 provides logic configured to (i) set a first status to an invalid state in response to a first data buffered in a first register being invalid. In contrast, both Mirapuri and Steiss appear to be silent regarding status for data registers. As argued above for claim 1, one of ordinary skill in the art of pipeline processors would distinguish between an instruction register and a data register per FIG. 4 of Mirapuri. With no status bits for data registers to set, no logic appears to exist in Mirapuri to set the non-existing status bits. Steiss does not appear to cure the defect of Mirapuri. Therefore, Mirapuri and

Steiss, alone or in combination, do not appear to teach or suggest logic configured to (i) set a first status to an invalid state in response to a first data buffered in a first register being invalid as presently claimed.

Claim 8 further comprises a logic configured to (ii) stall a processor in response to both (a) an instruction requiring the first data and (b) the first status being in the invalid state. The argument on page 13, paragraph 26aii of the Office Action appears to be reversing a cause and an effect. Column 10, lines 55-65 of Mirapuri appear to indicate that **a pipeline overrun causes a stall** with a consequence that data remaining in the pipeline may be incorrect. In contrast, the **data being invalid causes the stall** in the claim. Furthermore, both Mirapuri and Steiss appear to be silent, and the Office Action makes no arguments, that the stall is also caused by an instruction requiring the data considered to be invalid. Therefore, Mirapuri and Steiss, alone or in combination, do not appear to teach or suggest a logic configured to (ii) stall a processor in response to both (a) an instruction requiring the first data and (b) the first status being in the invalid state as presently claimed.

Furthermore, the Office Action fails to establish *prima facie* obviousness for lack of clear and particular evidence to combine the references. For example, the assertion on page 14, paragraph 26d of the Office Action that having status bits close to

the associated data bits would "correspond to some speedup because of the physical closeness of needed information." does not appear to be taught by either Mirapuri, Steiss or knowledge generally available to one of ordinary skill in the art. No evidence or convincing line of reasoning has been presented in the Office Action that the circuitry receiving the data from a particular data register is physically close to the circuitry receiving the status also stored in the particular data register. To argue that placing the data and status in the same particular data register would somehow result in a logical speedup is merely a conclusory statement. Therefore, *prima facie* obviousness to combine the references has not been established. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 10 provides logic configured to set a first status to an invalid state in response to receiving a second data from a second register having a second status in the invalid state. In contrast, both Mirapuri and Steiss appear to be silent regarding logic setting a status bit in a second data register. Furthermore, the Office Action appears to be arguing that the second status bit is copied from the first status bit which does not follow the language of the claim. Therefore, Mirapuri and Steiss, alone or in combination, do not appear to teach or suggest logic configured to set a first status to an invalid state in response to receiving a

second data from a second register having a second status in the invalid state as presently claimed. As such, claim 10 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 2 provides a step for setting a first status for a first register to an invalid state in response to a conditional store for first data in the first register. In contrast, page 9, paragraph 23b of the Office Action admits that Mirapuri does not disclose setting a status bit for a data register in response to a conditional store. Furthermore, Sites appears to be silent regarding setting a status bit in a register in response to a conditional store. The argument on page 9, paragraph 23c that a combination of two references somehow teaches a step where neither reference alone teaches the step or any part thereof appears to be invalid. Therefore, Mirapuri and Sites, alone or in combination, do not appear to teach or suggest setting a first status for a first register to an invalid state in response to a conditional store for first data in the first register as presently claimed.

Furthermore, the assertion on page 10, paragraph 23d that achieving data integrity is motivation to combine the references appears to be merely conclusory. No evidence is provided in the Office Action that Mirapuri lacks data integrity upon executing a store. Therefore, adding Sites to Mirapuri to "achieve data integrity upon executing a store" is speculation, not clear and

particular evidence of motivation. Claim 9 provides language similar to claim 2. As such, claims 2 and 9 fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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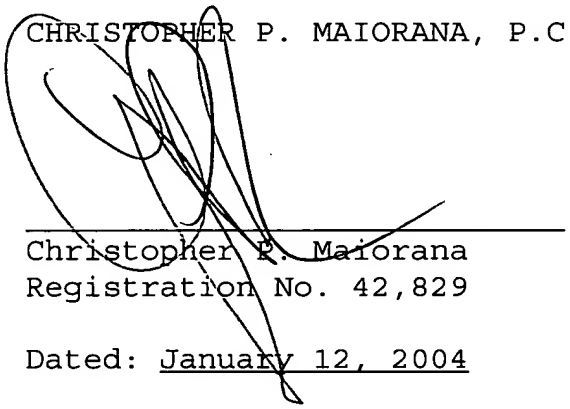

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